Simulation and Analysis of Two GaN MIS-HEMT-Based Step-down Level Shifters

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***Abstract*— In this paper, two step-down level shifter circuit structures based on AlGaN/GaN (aluminum-gallium-nitride/gallium-nitride) MIS-HEMTs (metal-insulator-semiconductor-high-electron-mobility-transistors) are proposed. The level shifter circuits have the capability to produce voltage drop. They are used to address the challenges of anomalous operation state in the sawtooth wave generator of PWM (pulse width modulation) integrated circuit, while also mitigating the undesirable device degradation resulting from high output voltage from the comparator. Proposed circuit structures are simulated and calibrated by ADS (Advanced Design System) platform. Additionally, calculations are carried out to analyze the principle of output voltage drop. Subsequently, the circuit output characteristics and parameter settings of these circuit structures are discussed, which offer insights and advice regarding their feasibility and the potential of step-down level shifter circuit structures for monolithically integrated GaN power converters.**

***Keywords*—AlGaN/GaN MIS-HEMTs, integrated circuits, Comparator, Step-down level shifter**

I. INTRODUCTION

AlGaN/GaN (aluminum-gallium-nitride/gallium-nitride)-HEMTs (high-electron-mobility-transistor) possess the advantages of fast switching performance, high-temperature operation, and large breakdown voltage, which enable them to be a potential candidate for the next generation of efficient power electronics [1-5]. Furthermore, the GaN-on-Si technology permits the monolithic integration of several devices for a compact structure that decreases the effect of parasitic characteristics on the circuit [6]. The AlGaN/GaN MIS-HEMTs (metal-insulator-semiconductor-high-electron-mobility-transistor) exhibit superior capabilities of low leakage current, scaling up threshold voltage, and wide gate voltage swing [7]. Within increased gate input tolerance, additional gate protection devices are not required thus reducing circuit complexity [8]. According to these advantages, the AlGaN/GaN MIS-HEMTs offer more effective and space-saving solutions for power conversion [9-10].

The comparator unit as the fundamental component of mixed-signal circuits has caught considerable attention [11]. Additionally, the comparator is a crucial component of the sawtooth generator, which is employed in pulse width modulation (PWM) circuits frequently [12-14]. Li et al. comprehensively investigated comparator characteristics, encompassing different temperatures and frequencies [15]. This study revealed that integrated comparators based on MIS-HEMTs exhibit both a large and stable comparison range, along with high voltage swings.

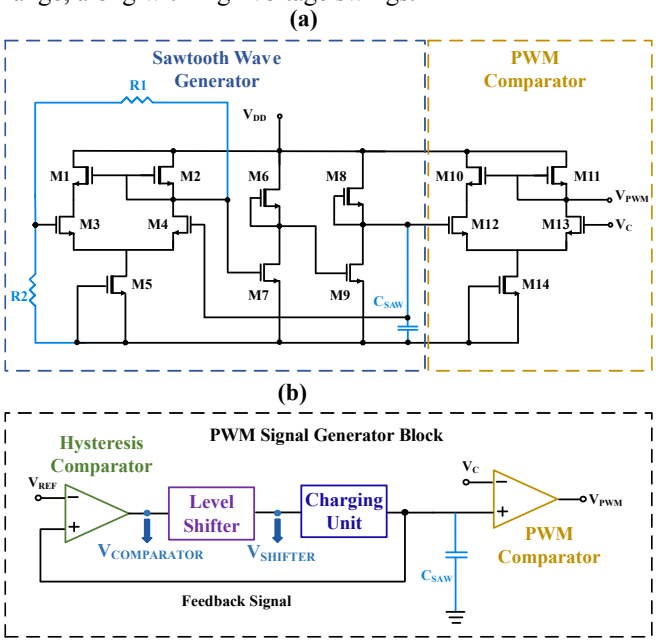

Fig. 1. (a) Schematic of PWM generator without level shifter circuit [17]; (b) Proposed PWM generator block diagram.

Despite its merits, the comparator generally has a logic-low voltage ranging from 3 to 5 V [16], posing challenges in achieving voltage signal recognition on the charging unit when employing a sawtooth generator in the PWM circuit shown in Fig.1 (a) [17]. Additionally, the output voltage's proximity to the 10 V supply voltage might cause undesirable device degradation [18]. The step-down level shifter circuit, demonstrated by Wang et al., was utilized in the PWM integrated circuit for GaN power converters as depicted in Fig.1 (b) [13]. This level shifter circuit using fluorine plasma ion implementation technique has an operating voltage from 0 to 4 V and it is used to shift down the comparator output voltage to a lower level. Besides, K. Fricke et al. also mentioned a resistor-based level shifter structure based on GaAs operation amplifier circuit [19].

In this work, two level shifter circuits based on AlGaN/GaN MIS-HEMTs are proposed with parameters analysis to optimize their performance. A comprehensive evaluation of the level shifter's performance is conducted through static and dynamic simulations using ADS (Advanced Design System) platform. The simulations are focused on optimizing the device parameters to enhance circuit performance, particularly concerning the output voltage and circuit overshoot current. Calculations for both

circuit structures are performed to validate the simulation results.

II. Simulation and Discussion

The level shifter circuits depicted in Fig. 2 encompass two distinct structures. The L-FER-based level shifter is configured in the form of the source follower, incorporating an additional lateral field-effect rectifier (L-FER) [20] to further decrease the output voltage level. On the other hand, the resistor-based level shifter also employs a source follower with a resistor being utilized to lower the output voltage.

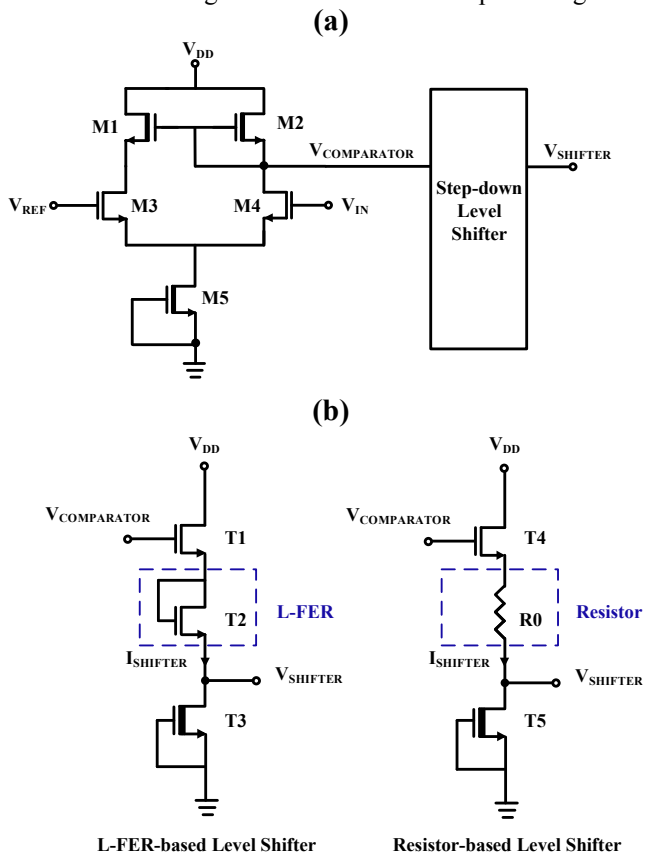

Fig. 2. (a) Schematic of simulation circuit; (b) L-FER-based level shifter and resistor-based level shifter.

The MIS-HEMT D/E-mode device parameters in the ADS platform are set based on previous research on GaN-based ASM (Advanced Spice Model)-HEMT conducted by Lu et al [21]. The open loop simulations with passive components disconnected are performed to analyze the static and dynamic performance. The simulation circuit is depicted in Fig. 2 (a), and relevant information is presented in TABLE I. The size of the comparator with chosen optionally.

TABLE I: Key parameters for the circuit simulation

Parameters	Values
Width of D-mode MIS-HEMTs $W_{D\text{-}mode}$ (μm)	M1 = M2 = 20 M5 = 25; T3 = 10
Width of E-mode MIS-HEMTs $W_{E\text{-}mode}$ (μm)	M3 = M4 = 20 T1 = T2 = 150
Voltage supply (V)	V_{IN} = 0 - 10
D-mode MIS-HEMTs (cut-off voltage in V)	-4
E-mode MIS-HEMTs (cut-off voltage in V)	2
Resistor R0 (kΩ)	1

A. Static simulation results of level shifter circuits

The static simulation results for $V_{SHIFTER}$ and $V_{COMPARATOR}$ are illustrated in Fig. 3, shift down voltage of output waveform can be noticed for both level shifter structures, the logic low output voltage of comparator is shifted down to voltage level close to 0 V. This phenomenon indicates that both structures possess the capability to voltage drop.

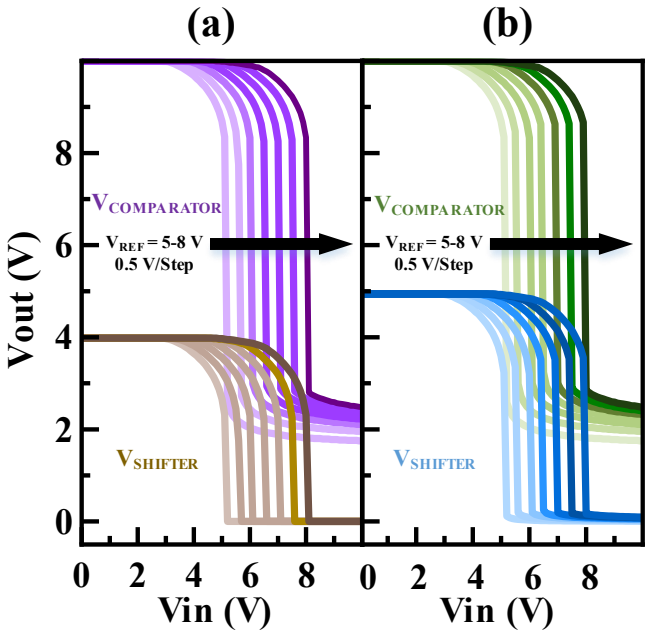

Fig. 3. The comparator output voltage and level shifter output voltage with the reference voltage from 5 V to 8 V with 0.5 V step (a) L-FER-based level shifter; (b) resistor-based level shifter.

B. Dynamic simulation results of level shifter circuits

In the dynamic simulation, a sawtooth AC signal with a voltage of 0 − 10 V and frequency of 100 kHz is introduced at the input port of the comparator. Fig. 4 illustrates the output characteristics of two step-down level shifters for different device sizes.

In the simulation of the L-FER-based level shifter, the impact of the width of E-mode HEMT on the level shifter circuit is investigated and the width ratio is defined as $W_{E\text{-}mode}$: $W_{D\text{-}mode}$. The results presented in Fig. 4 (a) indicate for a fixed width of D-mode HEMT, the smaller width of E-mode HEMT could potentially lead to a reduction in $V_{SHIFTER}$ to some extent.

Nevertheless, From Fig. 4 (b), minimal impact on the current in the level shifter circuit is observed that alterations under the width of E-mode HEMT from 50 to 1000 μm. This might primarily be attributed to the relatively small width of the D-mode device, where the maximum current in the circuit is predominantly limited by the saturation current of D-mode HEMT.

Regarding the output characters under different D-mode widths from 10 to 150 μm, the simulation result in Fig. 4 (c) and (d) indicates that higher width of D-mode HEMT would contribute to a larger voltage drop and an increased current in the level shifter, such phenomenon tends to diminish as D-mode width increases further.

Concerning the impact of both E-mode HEMTs and D-mode HEMTs, as depicted in Fig. 4, there emerges a

discernible connection between the output voltage of the L-FER-based level shifter and the ratio between the width of E-mode and D-mode HEMT. For instance, similar output voltage levels of approximately 4 V can be observed for cases where $W_{E\text{-mode}}$ = 300 µm, $W_{D\text{-mode}}$ = 20 µm and $W_{E\text{-mode}}$ = 150 µm, $W_{D\text{-mode}}$ = 10 µm. These devices exhibit a consistent width ratio of 15:1. Additionally, a large overshoot current is observed when employing a high E-mode and D-mode width ratio. This excessive overshoot may cause device damage [22]. A smaller width ratio is anticipated to mitigate the detrimental effects of overshoot.

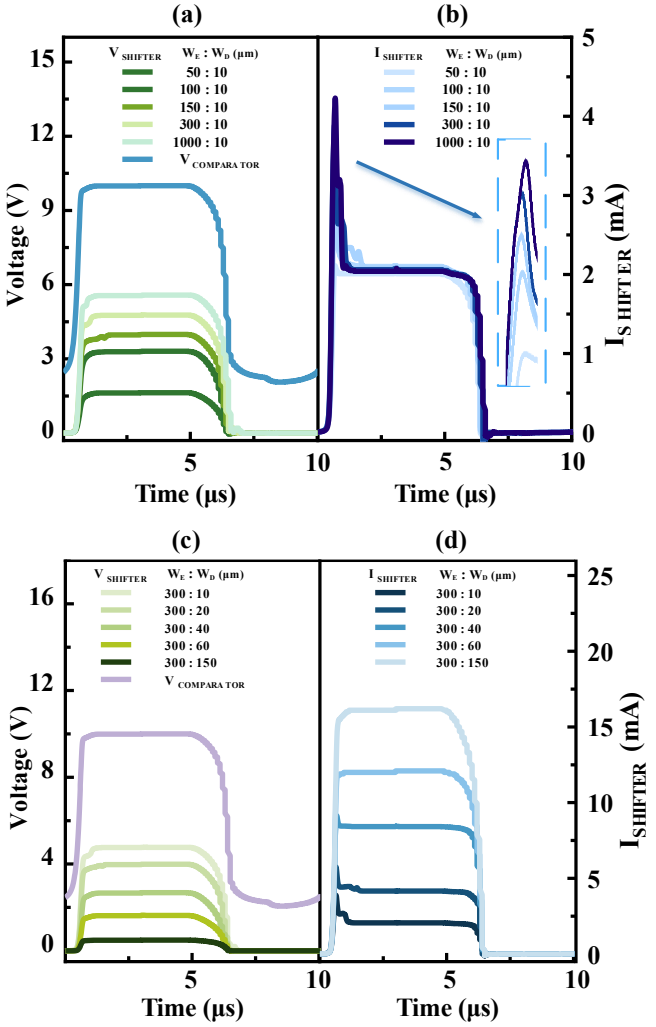

Fig. 4. (a) V_{out} and $V_{SHIFTER}$ with different E-mode width; (b) Level shifter current with different E-mode size; (c) V_{out} and $V_{SHIFTER}$ with different D-mode width; (d) Level shifter current with different E-mode size.

As simulation results of the Resistor-based level shifter depicted in Fig. 5, it can be observed that higher resistance is associated with a comparatively larger voltage drop. Additionally, increasing the resistance of R0 effectively mitigates overshoot current, and minor variations in $I_{SHIFTER}$ are observed across different resistance values.

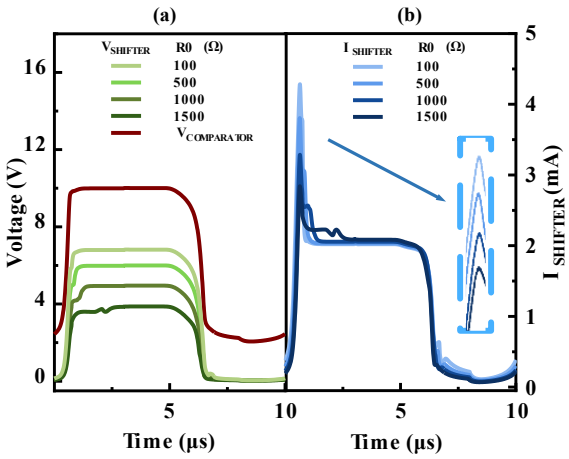

Fig. 5. (a) V_{out} and $V_{SHIFTER}$ with different resistance; (b) Level shifter current with different resistance;

III. Circuit Analyze of Level Shifter Structures

A. L-FER-based Level Shifter analyzes

In the circuit configuration of the L-FER-based level shifter depicted in Fig. 2 (b), the D-mode HEMT T3 also operates in the saturation region within its working region. By connecting its gate to the source terminal (V_{GS} = 0 V). The D-mode transistor exhibits a threshold voltage of about -4 V and the drain side maintains a higher voltage level compared to the magnitude of threshold voltage during its operation. As a consequence, the condition $V_{DS} > V_{GS} - V_{th}$ is satisfied, indicating that this D-mode transistor operates in the saturation region. Regarding the E-mode transistor T2, where the drain and gate are connected ($V_{GD} = 0$ V), the condition $V_{DS} > V_{GS} - V_{th}$ still holds since $V_{th,T2} > 0$. The E-mode transistor T2 will working in the saturation region. In reference to the MIS-HEMT model [23], the drain current is given by [24]:

$$I_{D,Sat} = \frac{1}{2}\mu_{eff} C_{eff} \frac{W}{L}(V_{GS} - V_{th})^2$$

Where μ_{eff} is the effective mobility, C_{eff} is the effective capacitance, and W/L is the width over length ratio. Devices T2 and T3 are supposed to work in saturation mode with the same current. Then, the following equation can be deduced:

$$V_{DS,T2} = V_{GS,T2} = |V_{th,T3}| \sqrt{\frac{k_{n,D}}{k_{n,E}}} \sqrt{\frac{W_{T3}}{W_{T2}}} + V_{th,T2}$$

Setting the $W_{T3}/W_{T2} = K_R$

$$V_{DS,T2} = V_{GS,T2} = \sqrt{k_{n,D}/k_{n,E}} * \sqrt{K_R} * |V_{th,T3}| + V_{th,T2}$$

Where $k_{n,E}/k_{n,D} = (\mu_{eff,E} * C_{eff,E})/(\mu_{eff,D} * C_{eff,D})$. The value of $V_{DS,T2}$ may be construed as the voltage drop across the L-FER. Similarly, the E-mode transistor T1 also have a roughly voltage drop of $V_{th,T1}$ when T1 opens in its expected voltage level. This calculation result further confirms previous simulation results. Firstly, when the width ratio W_{T3}/W_{T2} is increased, a larger voltage drop across L-FER would occur, resulting in a smaller output voltage. Secondly, the voltage drop across L-FER in the level shifter is influenced by the value of K_R, which aligns with the results obtained from the previous simulation. Several recommendations can be proposed for application, based on the calculation and simulation results. To achieve a fixed voltage drop on the input voltage, which implies that $V_{DS,T2}$ approaching constant

value, this requires larger W_{T2} / W_{T3} ratio value and smaller threshold voltage $V_{th,T3}$. This will contribute to the constant voltage drop of L-FER with its value approaching $V_{th,T2.}$ However, as mentioned in the simulation discussion, large W_{T2}/W_{T3} would result in the current overshoot. Therefore, trade-offs need to be considered on circuit performance between stable voltage drop and overshoot current.

B. Resistor-based level shifter analyzes

Regarding the resistor-based level shifter, the resistor is applied to further decrease the output voltage. Based on the similar circuit structure analysis proposed by [25]. The voltage drop across the resistor can be approximated by the following expression:

$$V_{R\,drop} \propto R * I_{SHIFTER}$$

Precise resistance is expected to achieve a predictable voltage drop. Larger resistance is recommended to mitigate current overshoot. Moreover, adjustments to the size of E-mode HEMT and D-mode HEMT devices can be employed to regulate circuit current ensuring a proper $V_{R\,drop}$. However, several factors also need to be taken into account including temperature which may affect the operation of the circuit.

IV. CONCLUSION

In conclusion, this study delves into two step-down level shifter circuits based on MIS-HEMT devices. Simulations were conducted to analyze the circuit performance concerning circuit overshoot current and output voltage. Additionally, the impact of the width ratio of devices on the output voltage and overshoot current is thoroughly discussed. Furthermore, the calculations and simulation results offer guidance for designing an optimized L-FER-based level shifter with predictable voltage drop and stable performance. Consequently, both structures are analyzed with regard to potential applications in future circumstances. This work contributes to application potential of level shifter designs and offers guidance for their integration into diverse circuit applications.

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REFERENCES

[1] K. J. Chen *et al*., "GaN-on-Si Power Technology: Devices and Applications," in *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 779-795, March 2017, doi: 10.1109/TED.2017.2657579.

[2] R. Gaska, Q. Chen, J. Yang, A. Osinsky, M. Asif Khan and M. S. Shur, "High-temperature performance of AlGaN/GaN HFETs on SiC substrates," in *IEEE Electron Device Letters*, vol. 18, no. 10, pp. 492-494, Oct. 1997, doi: 10.1109/55.624930.

[3] E. A. Jones, F. F. Wang and D. Costinett, "Review of Commercial GaN Power Devices and GaN-Based Converter Design Challenges," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707-719, Sept. 2016, doi: 10.1109/JESTPE.2016.2582685.

[4] D. Kinzer and S. Oliver, "Monolithic HV GaN Power ICs: Performance and application," in *IEEE Power Electronics Magazine*, vol. 3, no. 3, pp. 14-21, Sept. 2016, doi: 10.1109/MPEL.2016.2585474.

[5] C. -L. Tsai *et al*., "Smart GaN platform: Performance & challenges," *2017 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2017, pp. 33.1.1-33.1.4, doi: 10.1109/IEDM.2017.8268488.

[6] D. Kinzer, "GaN power IC technology: Past, present, and future," *2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, Sapporo, Japan, 2017, pp. 19-24, doi: 10.23919/ISPSD.2017.7988981.

[7] Z. Tang *et al*., "600-V Normally Off SiN_x /AlGaN/GaN MIS-HEMT With Large Gate Swing and Low Current Collapse," in *IEEE Electron Device Letters*, vol. 34, no. 11, pp. 1373-1375, Nov. 2013, doi: 10.1109/LED.2013.2279846.

[8] R. Gong *et al*., "AlGaN/GaN dual gate MOS HFET for power device applications," *2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology*, Shanghai, China, 2010, pp. 1353-1355, doi: 10.1109/ICSICT.2010.5667654.

[9] Y. Zhu, M. Cui, A. Li, F. Li, H. Wen and W. Liu, "Monolithic DFF-NAND and DFF-NOR logic circuits based on GaN MIS-HEMT," *2021 International Conference on IC Design and Technology (ICICDT)*, Dresden, Germany, 2021, pp. 1-4, doi: 10.1109/ICICDT51558.2021.9626401.

[10] M. Cui et al., "Monolithic integration design of GaN-based power chip including gate driver for high-temperature DC–DC converters," *Jpn. J. Appl. Phys*., vol. 58, no. 5, 2019, Art. no. 56505, doi: 10.7567/1347-4065/ab1313.

[11] A. M. H. Kwan, X. Liu and K. J. Chen, "Integrated gate-protected HEMTs and mixed-signal functional blocks for GaN smart power ICs," *2012 International Electron Devices Meeting*, San Francisco, CA, USA, 2012, pp. 7.3.1-7.3.4, doi: 10.1109/IEDM.2012.6478997.

[12] W. Wang, A. Li, M. Cui, H. Wen and W. Liu, "Monolithic Comparators using E/D-mode AlGaN/GaN MIS-HEMTs for High-temperature Applications," *2021 18th China International Forum on Solid State Lighting & 2021 7th International Forum on Wide Bandgap Semiconductors (SSLChina: IFWS)*, Shenzhen, China, 2021, pp. 33-35, doi: 10.1109/SSLChinaIFWS54608.2021.9675215.

[13] H. Wang, A. M. H. Kwan, Q. Jiang and K. J. Chen, "A GaN Pulse Width Modulation Integrated Circuit for GaN Power Converters," in *IEEE Transactions on Electron Devices*, vol. 62, no. 4, pp. 1143-1149, April 2015, doi: 10.1109/TED.2015.2396649.

[14] X. Li, M. Cui and W. Liu, "A full GaN-Integrated Sawtooth Generator based on Enhancement-mode AlGaN/GaN MIS-HEMT for GaN Power Converters," *2019 International Conference on IC Design and Technology (ICICDT)*, Suzhou, China, 2019, pp. 1-3, doi: 10.1109/ICICDT.2019.8790928.

[15] A. Li *et al*., "Monolithic Comparator and Sawtooth Generator of AlGaN/GaN MIS-HEMTs With Threshold Voltage Modulation for High-Temperature Applications," in *IEEE Transactions on Electron Devices*, vol. 68, no. 6, pp. 2673-2679, June 2021, doi: 10.1109/TED.2021.3075425.

[16] K. -Y. Wong, W. Chen and K. J. Chen, "Integrated voltage reference and comparator circuits for GaN smart power chip technology," *2009 21st International Symposium on Power Semiconductor Devices & IC's*, Barcelona, Spain, 2009, pp. 57-60, doi: 10.1109/ISPSD.2009.5158000.

[17] Y. Shen, Z. Li, A. Li and W. Liu, "Monolithically Integrated PWM Circuit Based on AlGaN/GaN MIS-HMETs for All-GaN Smart Power System," *2021 IEEE 14th International Conference on ASIC (ASICON)*, Kunming, China, 2021, pp. 1-4, doi: 10.1109/ASICON52560.2021.9620315.

[18] C. Ma et al., "ON-state critical gate overdrive voltage for fluorine implanted enhancement-mode AlGaN/GaN high electron mobility transistors," *J. Appl. Phys.*, vol. 110, no. 11, pp. 114514-1–114514-7, Dec. 2011

[19] K. Fricke, H. L. Hartnagel, W. Y. Lee and M. Schussler, "AlGaAs/GaAs/AlGaAs DHBT's for high-temperature stable circuits," in *IEEE Electron Device Letters*, vol. 15, no. 3, pp. 88-90, March 1994, doi: 10.1109/55.285393.

[20] K. J. Chen, "GaN smart power chip technology," *2009 IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC)*, Xi'an, China, 2009, pp. 403-407, doi: 10.1109/EDSSC.2009.5394230.

[21] S. Lu, K. Chen, J. Liu, P. Cui, A. Li and W. Liu, "Design and simulation of GaN devices and integrated circuits using ASM compact HEMT model for mixed-signal applications," *2022 19th China International Forum on Solid State Lighting & 2022 8th International Forum on Wide Bandgap Semiconductors (SSLCHINA: IFWS)*, Suzhou, China, 2023, pp. 61-64, doi: 10.1109/SSLChinaIFWS57942.2023.10071042.

[22] R. Katada *et al*., "Digital Gate Driving (DGD) is Double-Edged Sword: How to Avoid Huge Voltage Overshoots Caused by DGD for GaN FETs," *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, Vancouver, BC, Canada, 2021, pp. 5412-5416, doi: 10.1109/ECCE47101.2021.9595264.

[23] J. Zhang, B. Syamal, X. Zhou, S. Arulkumaran and G. I. Ng, "A Compact Model for Generic MIS-HEMTs Based on the Unified 2DEG Density Expression," in *IEEE Transactions on Electron Devices*, vol. 61, no. 2, pp. 314-323, Feb. 2014, doi: 10.1109/TED.2013.2295400.

[24] A. Li *et al*., "A Monolithically Integrated 2-Transistor Voltage Reference With a Wide Temperature Range Based on AlGaN/GaN Technology," in *IEEE Electron Device Letters*, vol. 43, no. 3, pp. 362-365, March 2022, doi: 10.1109/LED.2022.3146263.

[25] M. P. Kaufmann and B. Wicht, "Monolithic Integration in E-mode GaN Technology," *Synthesis Lectures on Engineering, Science, and Technology (SLEST)*.